The Chips Manufactured by the Students : News from the MOS Training Fab

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Abstract

Thanks to the introduction of the self-aligned polysilicon gate MOSFET, it becomes possible to introduce in the basic MOS device fabrication training the manufacturing of digital integrated circuits, while keeping the process as simple as before (4 masks). The results are rewarding, and result in a better matching between the VLSI design lectures and the fabrication training.

1. The Academic Semiconductor Fab

The clean room at A.I.M.E. (Atelier Interuniversitaire de Micro-électronique) was created to provide to a large number of students (more than 300 per year) a practical training on basic MOS device fabrication.
A high level of motivation is induced among the students by enabling them to obtain working devices at the end of one week, starting from a blank wafer.
The process must be kept very simple, to comply with two types of limitation : a reasonable equipment budget and the strictly limited duration of the process (1 week).
For instance, the number of photolithographic steps (mask levels) is only four.
The recent introduction of the self-aligned polysilicon gate opens new possibilities of integration, by bringing two improvements :
a) smaller and more efficient devices (10 micron channel length MOSFETs)
b) two insulated levels of interconnect (polysilicon and aluminium)
To highlight these possibilities, new sets of 4 masks have been made, mixing several characterization chips with more complex digital ICs, containing about 25 transistors per mm^2. The idea is to give a practical example showing that the basic resources of VLSI manufacturing are effectively present.
At the end of the process, these complex ICs go through a functional test, performed in parallel with the MOS devices characterization, that remains the main target of the training [1].

2. CAD tools involved

Taking into account parameters like mask fabrication accuracy, alignment tolerance and photoresist/ etching error, design rules were issued for the A.I.M.E. poly gate process. Based on these rules, a design kit for the “Cadence” tool was built, allowing DRC (design Rules Checking), LVS (Layout Versus Schematic comparison), and SPICE netlist extraction.

Table 1 : design rules

Single layer rules : width spacing Active Area : 20µ 20µ Poly gate : 10µ 20µ Contact : 20µ 20µ Aluminum : 20µ 20µ ***Contact overlap :*** Active Area : 10µ Poly gate : 10µ Aluminum : 6µ	***Two layers spacing :*** Poly - Act. Area : 6µ Contact - channel : 20µ ***Extension beyond channel :*** Poly : 10µ Active Area : 20µ

2.1 Design Rules

The layout design rules have to fulfill the following needs :
c) the rules must be compatible with the accuracy of the equipment (mask fabrication, alignment, photoresist, etching),
a) they must take into account the moderate quality of the work performed by the unexperienced users,
c) the rules must look like the most usual industrial rules, even if the scale is not the same.
The four mask levels are : Active Area, Polysilicon, Contact Opening, Aluminium Interconnect.
The creation of the rules is usually performed in an iterative manner : a preliminary set of rules is issued, and experimental results lead to rules update.
The first rules set (*table 1*) for the A.I.M.E polysilicon gate process was written in June 1995, based on the following parameters :
mask fabrication accuracy = 3 microns,
alignment accuracy = 2 microns,
photoresist and etching error = 2 microns
After 6 runs, the evaluation of the results obtained showed no urgent need to change these rules : a yield of about 95% is achieved for the simple devices, and 50% for the most "risky" chips.

A specific interface program was written to translate the layout files from a standrad format (CIF or GDS2) to the proprietary format of the mask making machine "Draftek" available at A.I.M.E.

2.2 Simulation Models

After fabrication of some wafers using a preliminary masks set, the SPICE model of the NMOS transistor (level 2) was manually extracted.
The first step is the introduction of parameters coming from the process knowledge, like :
- substrate doping, known from substrate resistivity measurements
- drain/source junction depth, measured on cross sections or oblique sections
- gate oxide thickness, measured by mechanical, optical or electrical means
- lateral diffusion, estimated from the electrical comparison between long and short channel transistors

The second step is the fine-tuning, where the fitting between the measured and simulated DC characteristic curves is iteratively improved, typically by adjusting the "extrapolated threshold" VT0.
"Worst case" models (max. oxide thickness, min. lateral diffusion, max. VT0) and "best case" models are used to verify that the complex cells have good chances to operate in any circumstances.
In chapter 5, we give an example of comparison between simulation and measurements in a complex case.

3. The Characterization Chips

Two characterization chips are present on the currently fabricated wafer.

The chip "p1b" (see *figure 1*) contains the following devices :
- two N-MOS transistors
- two MOS capacitors,
- a diode
- a diffused resistor.

Measurements on this chip are the main goal of the standard MOS training.
A computer controled wafer probing equipment allows fast evaluation of the yield on a complete wafer.

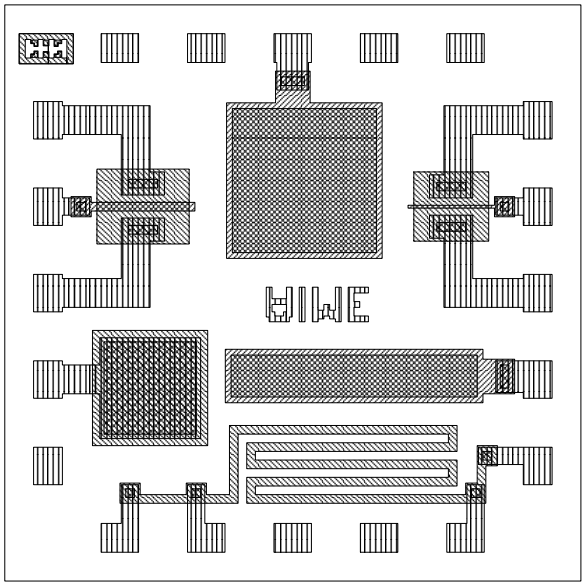

figure 1 : "p1b" chip

Some side effects are efficiently managed using pairs of devices.
For instance, the two MOS transistors of different lengths make possible an estimation of the channel length correction parameter, also known as “lateral diffusion”.
A similar strategy is used to obtain the value of capacitance per area unit, free of border effect, from the measurement of two capacitors which have the same perimeter but different areas.
On the upper left corner, the standard mask alignment pattern is visible.

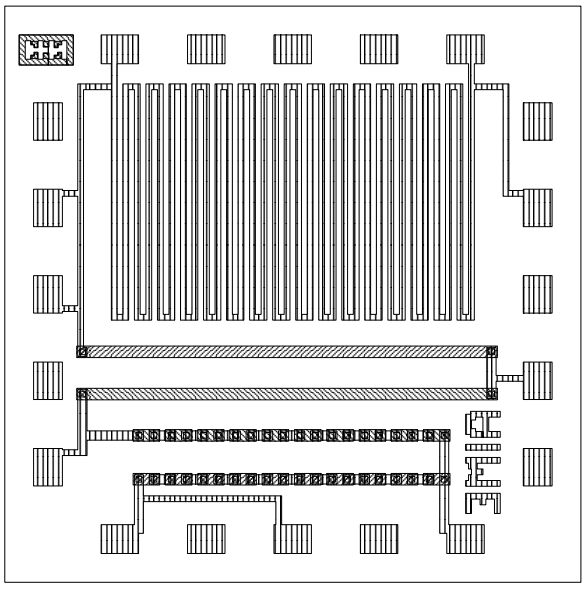

figure 2 : "p5b" chip

The chip "p5b" (see *figure 2*) contains only resistors. It allows accurate measurement of :
- sheet resistance of aluminium, polysilicon, N+ diffusion,
- contact resistance between aluminium and diffusion
- contact resistance between aluminium and polysilicon

Note that sheet resistances of poly and diffusion as well as contacts resistances are not measured directly. They are derived from the measurement of various strings made of contacts and resistive tracks.

Each measurement can be taken using 4 terminals for eliminating the parasitic effect of access resistance.

Like the other chips of our wafers, these chips occupy a space of 2 millimeters by 2 millimeters.
The bonding pads layout is standardized, allowing the wafer level testing (before cutting and encapsulating) of all chips with the same probe fixture.

4. The Digital Chips

The digital cells are based on a NOR gate (see *figures 3 and 4*) made only of enhancement MOS transistors. It is similar to the classical NMOS gate, with the difference that the passive pullup transistor is biased by a constant voltage instead of having the gate tied to the source.
In this configuration, the relative sizing of the pull-down and pull-up transistor is even more critical than in conventional NMOS [2].

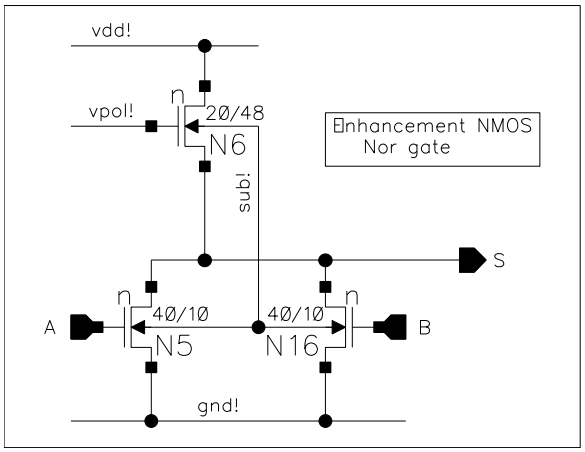

figure 3 : NOR schematic

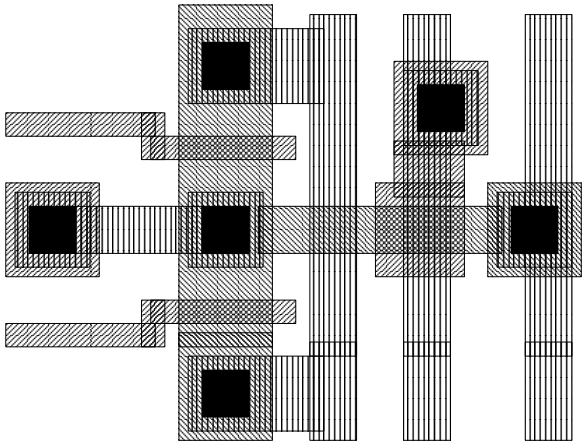

figure 4 : NOR layout

This constant bias (`vpol!` on *figure 3*) can be equal to the positive supply `vdd!`, but we also experienced the possibility of making it different (see chapter 5).
With the first set of masks, it appeared that the voltage gain of the digital gates in the worst case was only a little more than unity, and after further analysis with the HSPICE simulator, it was decided to improve it by increasing the pull-up transistor length (from 38 to 48 microns).

Based on enhancement NMOS NOR gates, three digital modules are proposed for experimentations, in order of increasing difficulty :

a) combinatorial circuit : a 2-to-4 decoder,
b) sequential circuit : an edge-triggered “D” flip-flop
c) feedback circuit : a Schmitt trigger

The "p2b" chip (see figure 5) contains these three modules, each one with independant input and output pads allowing separate testing. On the leftmost side, one can see the big L-shaped output transistors of the decoder, sinking current enough to drive directly some LEDs.
The inputs are protected against ESD (electro-static discharges) by a passive N-MOS transistor with the gate tied to the ground.

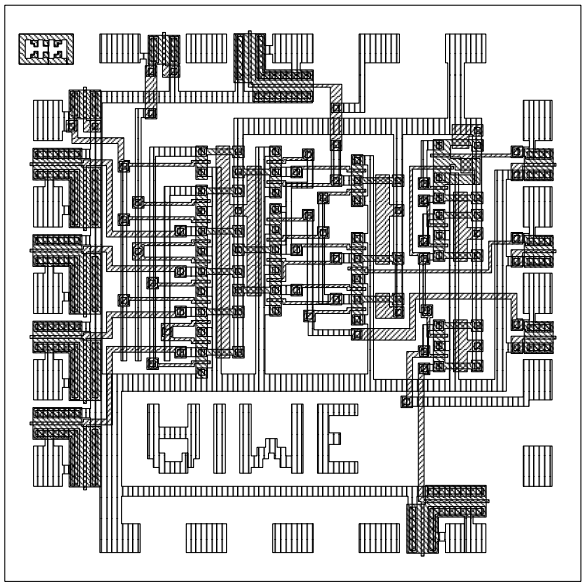

figure 5 : "p2b" chip

The “gadget” chip "p3b" contains the same three modules, cascaded in such a way that, with only the addition of an external capacitor and an external resistor, it drives in a cyclic way 4 LEDs or the 4 phases of a small stepping motor. This chip was presented in operation in various exhibitions [3],[4].

5. The Ring Oscillator

The traditional way of measuring the speed performance of digital cells is the ring oscillator, made of a an odd number of inverters. It offers an indirect evaluation of the typical inverter delay, in a simpler and more accurate way than any direct measurement.

Our modest N-MOS process does not pretend to participate to the silicon worldwide speed competition, but we had to propose a demonstration of this academic exercise.

The chip "p4b" (see *figure 6*) contains a ring oscillator made of 24 inverters and a NOR gate. The purpose of the NOR gate is to allow an external control of the starting of the oscillation. (Otherwise, the oscillator could start on a "multiple" frequency.)

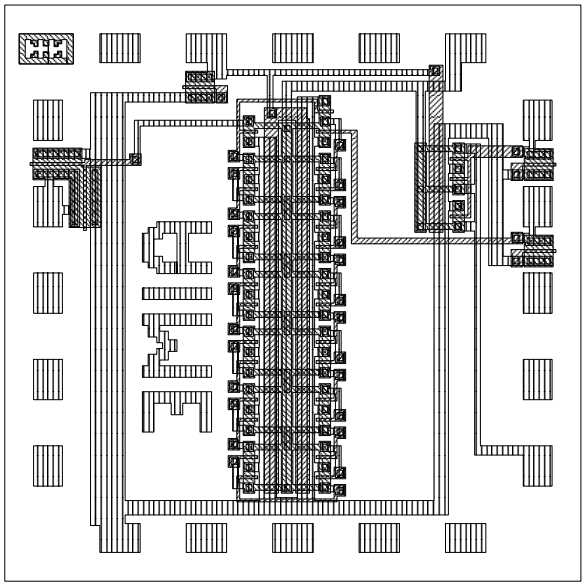

figure 6 : "p4b" chip

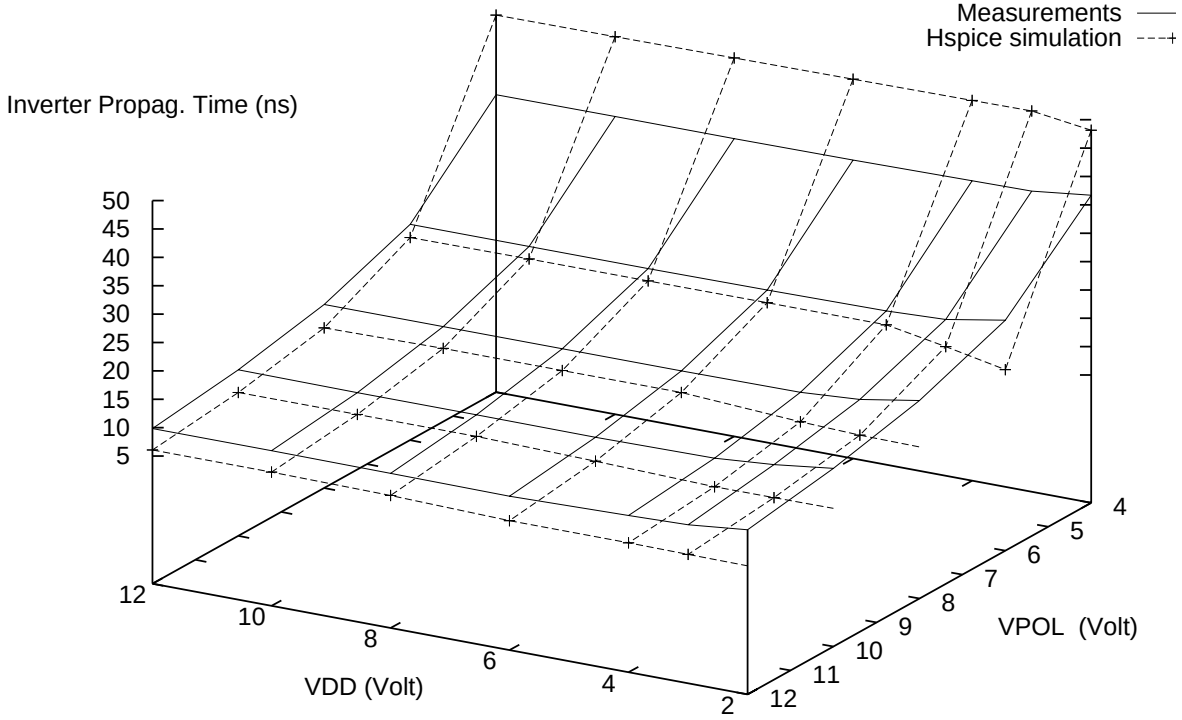

figure 7 : measurement vs simulation

This chip allows a separate control of "vpol" (pull-up gate bias) and "vdd" (pull-up drain power supply). Observing the oscillation frequency while varying these two voltages led our students to the surprising conclusion that "vdd" has a very little influence on the inverter propagation delay.
To eliminate the hypothesis of a wrong experimental procedure, we verified this property by simulation. (Like in the actual experiment, the inverter delay was estimated from the oscillator frequency.)
The results (see *figure 7*) show a very satisfying agreement between simulation and measurement, specially where the "vdd" sensitivity is concerned.
Note that on the right side of the 3-D diagram, a few simulated points are missing : this is due to the fact that the simulated circuit refused to oscillate, where the actual circuit accepted to work !
This denotes that our Spice models are not perfect and need some more refining.

Conclusion

Working in an academic semiconductor fab is very rewarding, and the fact that we cannot compete with the sub-micronic state-of-the-art is not really a problem.
Students are very motivated by the practical illustration of what they learn in the VLSI lectures, and this helps a lot understanding the trends in technology and CAD.
A single university or engineers school could not support the high cost of maintaining a semiconductor fab, but sharing the expense between a great number of institutions makes it acceptable.
The introduction of microsystems will be the next step of the evolution of this activity.

References

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