# INTRODUCING DIGITAL GATES IN THE BASIC MOS FABRICATION TRAINING

Jean Louis NOULLET, Pierre-François CALMON, Guy PIERREL,
Philippe BOURDEU d'AGUERRE
*A.I.M.E. - Campus INSA - Complexe Scientifique de Rangueil*
*31077 TOULOUSE*
*tel (33) 61 55 99 62, fax (33) 61 55 99 09, email noullet@aime.insa-tlse.fr*

Thanks to the introduction of the self-aligned polysilicon gate MOSFET, it becomes possible to introduce in the basic MOS device fabrication training the manufacturing of digital integrated circuits, while keeping the process as simple as before (4 masks). The results are rewarding, and result in a better matching between the VLSI design lectures and the fabrication training.

## 1. Presentation of the Academic Semiconductor Fab

The main goal of the process clean room at A.I.M.E. (Atelier Interuniversitaire de Micro-électronique) is to provide to a large number of students (more than 300 per year) a practical training on basic MOS device fabrication.

A high level of motivation is induced among the students by enabling them to obtain working devices at the end of one week, starting from a blank wafer.

The process must be kept very simple, to comply with two types of limitation : reasonable equipment budget and strictly limited duration of the process (1 week).

For instance, the number of photolithographic steps (mask levels) is only four, and for many years the standard chip, containing 2 MOS (aluminium gate) transistors, a MOS capacitor, a diode and a resistor, was viewed as sufficiently complex.

Nevertheless, the recent introduction of the self-aligned polysilicon gate opens new possibilities of integration, by bringing two improvements :

a) smaller and more efficient devices (10 micron channel length MOSFETs)

b) two insulated levels of interconnect (polysilicon and aluminium)

To highlight these possibilities, new sets of 4 masks have been made, mixing the standard chips with more complex digital ICs, some containing about 25 transistors per $mm^2$. The idea is to give a practical example showing that the basic resources of VLSI manufacturing are effectively present.

At the end of the process, these complex ICs go through a functional test, performed in parallel with the MOS devices characterization, that remains the main target of the training [1].

## 2. Design Rules

The layout design rules have to fulfill the following needs :

c) the rules must be compatible with the accuracy of the equipment (mask fabrication, alignment, photoresist, etching),

a) they must take into account the moderate quality of the work performed by the unexperienced users,

c) the rules must look like the most usual industrial rules, even if the scale is not the same.

The creation of the rules is usually performed in an iterative manner : a preliminary set of rules is issued, and experimental results lead to rules update.

The first rules set (table 1) for the A.I.M.E polysilicon gate process was written in June 1995, based on the following parameters :

mask fabrication accuracy = 3 microns,

alignment accuracy = 2 microns,

photoresist and etching error = 2 microns

Table 1 : design rules

***Single layer rules :***

| | width | spacing |
|---|---|---|
| Active Area : | 20µ | 20µ |
| Poly gate : | 10µ | 20µ |
| Contact : | 20µ | 20µ |
| Aluminum : | 20µ | 20µ |

***Contact overlap :***

| | |
|---|---|
| Active Area : | 10µ |
| Poly gate : | 10µ |
| Aluminum : | 6µ |

***Two layers spacing :***

| | |
|---|---|
| Poly - Act. Area : | 6µ |
| Contact - channel : | 20µ |

***Extension beyond channel :***

| | |
|---|---|
| Poly : | 10µ |
| Active Area : | 20µ |

After 6 runs, the evaluation of the results obtained showed no urgent need to change these rules : a yield of about 95% is achieved for the simple devices, and 50% for the most "risky" chips.

## 3. Mask Drawing and Fabrication

Masks are drawn at A.I.M.E. using the professional CAD tool "Cadence", run on Unix worstations, with the proper configuration to allow automated verifications, which are : DRC (Design Rules Checking), and LVS (Layout Versus Schematic comparison).

The mask-making machine (Draftek) is intented to discrete device fabrication rather than for ICs, and for this reason uses a proprietary data format.

Thus, the layouts have to be translated from a standard layout format (CIF or GDS2) to the "draftek" format, using a specific program that was written at A.I.M.E..

## 4. Digital Gates

The digital cells are based on a NOR gate (fig. 1) made only of enhancement MOS transistors. It is similar to the classical NMOS gate, with the difference that the passive pullup transistor is biased by a constant voltage instead of having the gate tied to the source.

In this configuration, the relative sizing of the pull-down and pull-up transistor is even more critical than in conventional NMOS [2].

With the first set of masks (fig. 2), it appeared that the voltage gain of the digital gates was only a little more than unity, and after analysis with the HSPICE simulator, it was decided to improve it by increasing the pull-up transistor length (from 38 to 48 microns).

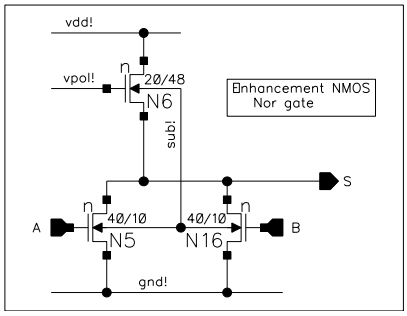


Figure 1 : NOR schematic

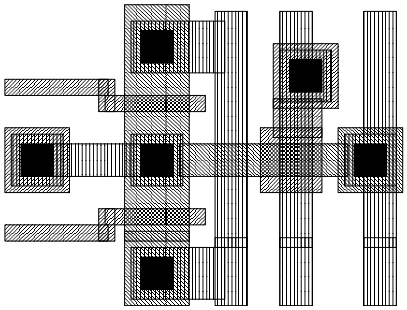

Figure 2 : NOR layout

## 5. Digital Chips

Three digital modules are proposed for experimentations, in order of increasing difficulty :

a) combinatorial circuit : a 2-to-4 decoder,

b) sequential circuit : an edge-triggered "D" flip-flop

c) feedback circuit : a Schmitt trigger

The chip known as "puce p2b" contains the three modules with independant input and output pads for separate testing, while another chip called "puce p3b" contains the three modules interconnected as follows :

- the clock input of the flip flop receives the output of the Schmitt trigger
- the D input of the flip-flop receives the Qb output of the same flip-flop, to form a simple binary counter
- the 2-to-4 decoder receives as least significant bit the clock of the flip-flop, and as most significant bit the Q output of the flip-flop.

This way, if the input of the trigger is fed with a periodic signal, the four outputs of the decoder will be activated one by one in a cyclic sequence. In addition, it is possible to use the trigger as an oscillator, by feeding back its inverted output by means of an external RC network.

Fig. 3 shows the layout of "puce p2b", that fits in a 2mm by 2mm die. On the left side is the decoder, in the middle the flip-flop and on the right side the Schmitt trigger.

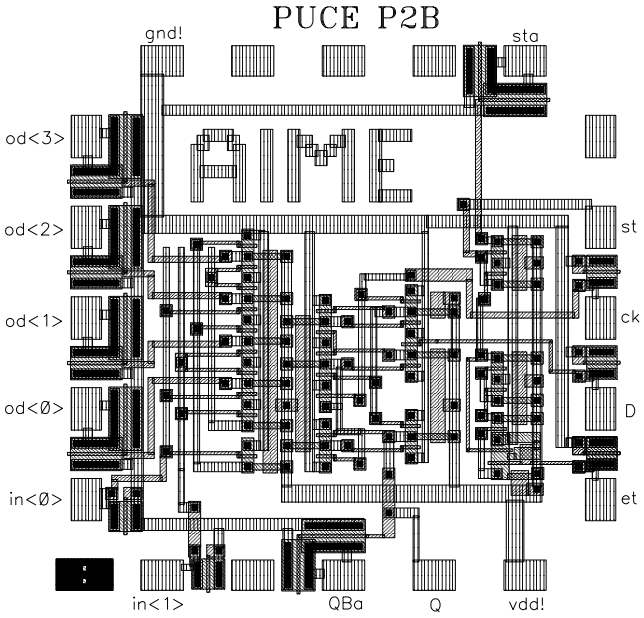

Fig. 3 : chip "puce p2b"

On the leftmost edge, one can see the wide L-shaped transistors used for the decoder ouputs, providing enough current for 4 LEDs or the 4 phases of a small stepping motor.

## 6. First Experimental Results

After 6 runs, it appeared that the best results were obtained by the decoder, that worked fine on most of the chips. The flip-flop worked on a little more than 50% of the chips, this indicating that it is more process sensitive. The trigger failed, behaving like an inverter without hysteresis. After analysis with more accurate HSPICE models, the conclusion was that the feedback loop gain of the trigger was too weak. This design mistake is corrected in the mask set presently being fabricated.

Most of the chips accept any supply voltage between 6V and 10V.

## References

[1] P.F. Calmon, G. Pierrel, "Caractérisation et test de composants. Automatisation de banc de mesures à partir du logiciel Labview", Troisièmes Journées Pédagogiques du CNFM, Saint Malo (France), Dec. 1994.

[2] C. Mead, L. Conway, "Introduction to VLSI systems", Addison-Wesley, 1980, page 20.